UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,420	01/27/2004	Jayesh R. Bhakta	NETL.001DV4	2206

20995 7590 08/19/2004

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,420	BHAKTA ET AL.	
	Examiner	Art Unit	
	Ly D Pham	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *040104 & 052804*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Pre-Amendment filed in March 01, 2004 has been entered.

2. Claims 1 – 20 are presented for the examination.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 claims the memory module of claim 1 wherein serpentine trace portions are absent from the first plurality of data lines. This claim is simply not understood. What are serpentine trace portions? And if the prior arts do not disclose such trace portions, would that be considered absent from the module, much less from the first data lines?

Clarification/explanation is required in order to overcome this type of rejection.

Claim 20 recites the limitation "the first lateral half" and "the second lateral half" in lines 3 – 4. There is insufficient antecedent basis for this limitation in the claim. Should claim 20 be dependent on claim 19 as opposed to claim 17?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 4 – 6, 8 – 12, and 17 – 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamasaki et al. (US Pat 6,594,167 B1).

Regarding **claims 1, 2, 8, 9, 17, and 18**, Yamasaki et al. disclose a memory module comprising:

a PCB having an edge , a first side, and a common signal trace connector area positioned long the edge (figs. 13 or 14, module 10 with top edge along the length, the module is shown with one side, and a common signal trace connector along the edge 12);

a first row of IC identical to one another (figs. 13 or 14, ICs 1A – 1I), the first row mounted on the first side of the PCB, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the ICs of the first row having a first orientation;

a second row of ICs identical to the ICs of the first row (figs. 13 or 14, ICs 1J – 1R identical to ICs 1A – 1I), the second row mounted on the first side of the PCB, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is the first row (figs. 13 or 14, top ICs are farther from the trace connector 12 than the bottom ICs), the ICs of the second row having a second orientation direction different from the first

orientation direction (figs. 13 or 14, the ICs on top are oriented 180 degrees from the bottom ICs);

a first plurality of data lines electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area (figs. 13 or 14, data lines connecting data pins DP to the trace connector area 12); and

a second plurality of data lines electrically connecting data pins of the second row of integrated circuit to the common signal trace connector area, whereby lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same (figs. 11A/11B, data pins portion of the ICs are positioned along the center line L1 of figs. 13 or 14, yielding substantial same data lengths to the common signal trace connector area. See also abstract: 'interconnections between the respective memory chips and the connect pins have substantially equal lengths').

Regarding **claims 4 – 6, 10 – 12, and 19**,Yamasaki et al. further show in figs. 13 or 14 the memory module having 8 ICs on each row per side of the PCB, hence a line of bilateral symmetry perpendicular to the edge and bisects the PCB into a first lateral half and second lateral half would be the line orthogonal to the long edge and crosses the edge's midpoint. Consequently, both the first and second rows are bilaterally symmetric with respect to the line of bilateral symmetry, per figs. 13, 14, or 19.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7, 13 – 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. in view of Perego et al. (US Pat 6,502,161 B1).

Regarding **claims 7, 13 – 16, and 20**, Yamaksaki et al. disclose the memory module of claim 4, wherein a set of address signal paths connecting the ICs of the first row and the second row on the first lateral half, a set of address signal paths connecting the ICs f the first row and the second row on the second lateral half, to a memory controller (figs. 2, 3, and 4), except a first common register for the ICs on the first lateral half, a second common register for the ICs on the second lateral half. In stead of having two separate chips, Perego et al. have disclosed a buffer for accessing the ICs in a combined fashion (fig. 4C, buffer 405), which means a single chip buffering the two rows of ICs. For the identical and practical purposes of addressing the memory chips, semiconductor fabrication for circuit combination is common and well known in the art to optimize space. Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to realize the variations of design from the scope disclosed by Perogo et al. as exemplified by the claimed features, all of which can be viewed as slight modifications in accordance with design preferences.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

11. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

12. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Ly Pham

August 16, 2004